accessing at least one of said plurality of groups of redundancy data cells and redundancy address cells;

detecting a redundancy address match condition for each of said accessed groups, wherein the redundancy address of said accessed group of redundancy address cells matches one of a plurality of inputted addresses; and

outputting redundancy data from said accessed group of redundancy data cells and redundancy address cells when said redundancy address match condition is detected.

97. The defect management engine as recited in claim 96 further comprising the step of overriding with new data said accessed group of redundancy data cells when said redundancy address match condition is detected.--

REMARKS

By this Preliminary Amendment, the original parent application claims are being canceled and a new set of claims being substituted. New claims 63-97 are respectively copies of claims 1-3, 5, 7-9, 14-16, 18, 20-21, 25-27, 31-35, 37, 39-46, 48 and 50-53 of U.S. patent no. 6,141,267 - Kirihata *et al.* (2000). The new claims are directed to defect management, such as described in the "Defect Mapping" section of the present application beginning on page 14, line 13. A copy of the Kirihata *et al.* patent is being filed with this Amendment for the convenience of the Examiner.

An early examination and allowance of the present application are solicited.

EXPRESS MAIL LABEL NO:

EL 873331478 US

Respectfully submitted,

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DETAILS OF CHANGES TO THE SPECIFICATION TEXT

Page 11, line 23 - page 12, line 5:

Optimized erase implementations have been disclosed in two copending U.S. patent applications. They are copending U.S. patent applications, Serial No. 204,175, filed June 8, 1988, by Dr. Eliyahou Harari, now patent no. 5,095,344, and one entitled "Multi-State EEprom Read and Write Circuits and Techniques," [filed on the same day as the present application] Serial No. 07/337,579, filed April 13, 1989, now abandoned, by Sanjay Mehrotra and Dr. Eliyahou Harari. The disclosures of the two applications are hereby incorporate by reference. The Flash EEprom cells are erased by applying a pulse of erasing voltage followed by a read to verify if the cells are erased to the "erased" state. If not, further pulsing and verifying are repeated until the cells are verified to be erased. By erasing in this controlled manner, the cells are not subject to over-erasure which tends to age the EEprom device prematurely as well as make the cells harder to program.

Page 22, lines 8 - 23:

After the bytes for a write cycle have been loaded into the selected memory device, the controller issues a program command to the memory device and initiate a write cycle. Optimized implementations of write operation for Flash EEprom device have been disclosed in two previously cited co-pending U.S. patent applications, Serial No. 204,175, now patent no. 5,095,344, and one entitled "Multi-State EEprom Read and Write Circuits and Techniques," Serial No. 07/337,579, filed April 13, 1989, now abandoned. Relevant portions of the disclosures are hereby incorporated by reference. Briefly, during the write cycle, the controller applies a pulse of programming (or writing) voltages. This is followed by a verify read to determine if all the bits have been programmed properly. If the bits did not verify, the controller repeats the program/verify cycle until all bits are correctly programmed.

Page 25, line 32 - page 26, line 11:

In the present invention, a system of Flash EEprom is used to provide non-volatile memory in place of traditional system memories such as disk storage. However, Flash EEprom memory is subject to wearing out by excessive program/erase cycles. Even with the improved Flash EEprom memory device as disclosed in co-pending U.S. patent applications, Serial No. 204,175, now patent no. 5,095,344, and one entitled "Multi-state EEprom Read and Write Circuits and Techniques," by Sanjay Mehrotra and Dr. Eliyahou Harari, Serial No. 07/337,579, filed April 13, 1989, now abandoned, [filed on the same day as the present application,] the endurance limit is approximately 10^6 program/erase cycles. In a ten-year projected life time of the device, this translates to a limit of one program/erase cycle per 5 minutes. This may be marginal in normal computer usage.